Amendments to the Specification

Please amend paragraph 0009 of the specification as originally filed as follows:

[0009] In a first embodiment of the invention, the computer ~~system~~ systems are arranged in a non-hierarchical configuration. A master sync signal is provided to both computer systems by a master sync signal generator or the like (which can be, for example, any video source). Each computer system includes synchronizing means that receives the master sync signal and causes the computer system to synchronize its output to this master sync signal.

Please amend paragraph 0011 of the specification as originally filed as follows:

[0011] This ~~second~~ first embodiment of the invention is adapted for synchronizing the display of video images generated by the two computer systems.

Please amend paragraph 0032 of the specification as originally filed as follows:

[0032] Sync separator 302 receives the master sync signal (e.g., a video signal) and extracts a sync or master pulse stream 303. Video and other extraneous information are removed. Master pulse stream 303 represents horizontal sync pulses (i.e., line rate rather than pixel rate). Master pulse stream 303 is then provided to phase detector 304. Phase detector 304 compares master pulse stream 303 to a slave pulse stream 305 received from rate controller circuit 314 and generates a difference pulse stream having pulses of varying widths representing a difference between the compared signals. LPF 306 low-pass filters the difference pulse stream to produce an analog voltage. The analog voltage is then input to VCO 308, where it controls the oscillation frequency of ~~the~~ VCO 308. The output of ~~the~~ VCO 308 is a video clock signal 309 that is fed to video generator 310. Video clock signal 309 is also fed back to rate controller circuit 314.

For the convenience of the Examiner and the Patent And Trademark Office, Applicants remind the Examiner that in the Reply To Office Action dated November 3, 2006, paragraph 0036 of the specification as originally filed was amended as follows:

[0036] In the 720 pixel per line example set forth above, rate controller 316 could initially set the divisor value to 720. If slave pulse stream 305 starts to lag master pulse stream 303, this will be detected by digital comparator 312 which would increase the value of the difference signal being provided to rate controller 316. In response, rate controller 316 will decrease the divisor to a value of, say, 710. This will cause pulses from divider 318 to arrive at phase detector 304 sooner than before. This, in turn, will cause VCO [[306]] 308 to slow down, effectively decreasing the response time of the loop. Similarly, if slave pulse stream 305 starts to lead master pulse stream 303, this will be detected by digital comparator 312 which would decrease the value of the difference signal being provided to rate controller 316. In response, rate controller 316 will increase the divisor to a value of, say, 730. This will cause pulses from divider 318 to arrive at phase detector 304 later than before. This, in turn, will cause VCO [[306]] 308 to speed up, effectively increasing the response time of the loop.

Amendments were also made to paragraph 0015 of the specification as originally filed, in the Reply To Office Action dated November 3, 2006. A further amendment was made to paragraph 0017 of the published application, which corresponds to paragraph 0015 of the specification as originally filed, in the Reply To Office Action dated December 10, 2007. Together, these amendments reflect the following changes to paragraph 0015 of the specification as originally filed:

[0015] Another aspect of the invention is the phase-locked loop circuit having a digital rate controller. The digital rate controller feature allows the phase-locked loop to be programmable so that its speed can be adjusted to react more ~~more~~ quickly or more slowly to changes.